The Claims Defining the Invention are as Follows

1. A method for forming an automatically passivated n-p junction, comprising the steps of:

providing a p-type body containing Group II and Group VI elements, one of which is mercury;

forming a passivation layer having at least one window provided therein on a surface of the p-type body;

subjecting said p-type body to a reactive ion etching process using the passivant layer as a mask to form the n-p junction; and

forming ohmic contacts to the n-type and p-type regions.

2. A method as claimed in claim 1, wherein the p-type body comprises mercury cadmium telluride.

3. A method as claimed in claim 1 or 2, wherein the step of forming a passivation layer with windows provided therein further comprises the steps of:

forming a passivation layer on the p-type body; and

etching windows therein.

4. A method as claimed in any one of the preceding claims, wherein the passivation layer has a thickness of 0.3 μm or less.

5. A method as claimed in any one of the preceding claims, wherein the passivation layer comprises ZnS.

6. A method as claimed in any one of the preceding claims, wherein the passivation layer comprises a first material underlying a second material wherein the second material is subsequently removed.

7. An n-p junction formed according to the method as claimed in any one of claims 1 to 6.

8. A method for forming an array of n-p junctions on a semiconductor body having a plurality of p-type material layers containing Group II and Group VI elements, one of which is mercury, comprising the steps of:

etching the body to expose a portion of each layer;

forming a passivation layer over the body;

forming a window in the passivation layer in each portion;

subjecting the body to a reactive ion etching process using the passivation layer as a mask to form an n-p junction in each layer;

forming an ohmic contact to each of the n-type regions; and

forming an ohmic contact to a common p-type layer.

9. A method as claimed in claim 8, wherein the step of etching the body exposes a plurality of portions within each layer at spaced locations across the body, to form a plurality of multi-wavelength detectors.

10. A method as claimed in claim 8 or 9, wherein the method further includes the step of etching a channel between adjacent detectors.

11. A method as claimed in claim 10, wherein said channel passes through all of the p-type layers except the common p-type layer.

12. A method for forming an array of n-p junctions on a semiconductor body having a plurality of p-type material layers containing Group II and Group VI elements, one of which is mercury, comprising the steps of:

etching the body to expose a portion of each layer;

forming a passivation layer over the body;

forming a window in the passivation layer;

subjecting the body to a reactive ion etching process to form n-p junctions that extend substantially to the substrate;

forming an ohmic contact to each of the common n-type regions; and

forming ohmic contacts to each layer on said portions.

13. A method as claimed in claim 12, wherein the step of etching the body exposes a plurality of portions of each layer at spaced locations across the body to form a plurality of detectors.

14. A method as claimed in claim 12 or 13, wherein adjacent detectors are separated by an n-p junction.

15. A semiconductor body comprising an array of n-p junctions formed thereon in accordance with the method as claimed in any one of claims 8 to 14.

16. A semiconductor material comprising an n-p junction, wherein the semiconductor material includes:

a substrate;

a layer of p-type material surmounting said substrate;

a region of converted n-type material formed on a localised portion of the surface of said p-type material, defining an n-p junction between the p-type and n-type material;

a passivation layer surmounting the surface of the p-type material and the n-p junction, including windows respectively exposing part of the surface of the converted n-type material and a portion of the surface of the p-type material distant from the n-type material for disposing ohmic contacts on the respectively exposed surfaces, without exposing the n-p junction.

17. A semiconductor material as claimed in claim 16, wherein the semiconductor material further includes ohmic contacts so as to form an electronically connectable component.

18. A semiconductor material as claimed in claim 16 or 17, wherein the p-type material is mercury cadmium telluride.

19. A semiconductor material as claimed in any one of claims 16 to 18, wherein the conversion is performed via a plasma induced process.

20. A semiconductor material as claimed in claim 19, wherein the plasma induced process is a reactive ion etching process that creates a laterally displaced n-on-p junction beneath the surface of the passivation layer, without degrading the passivation layer.

21. A semiconductor material as claimed in any one of claims 16 to 20, wherein the passivation layer is formed of zinc sulphide.

22. A semiconductor material as claimed in any one of claims 16 to 21, wherein the passivation layer has a thickness of 0.3μm.

23. A semiconductor material as claimed in any one of claims 16 to 22 wherein the material further includes a layer of n-type material interposed between said substrate and said layer of p-type material, such that said p-type layer surmounts said n-type layer, and said n-type layer surmounts said substrate to form a junction isolated n-on-p diode.

24. A semiconductor material as claimed in claim 23, wherein the region of n-type material extends through said p-type layer to said n-type layer.

25. A semiconductor material as claimed in claim 24, wherein said region of n-type material is annular, and is arranged to circumscribe a portion of said layer of p-type material so as to isolate the circumscribed portion from the remainder of said layer of p-type material.

26. A semiconductor material as claimed in claim 25, wherein a plurality of discrete regions of n-type material are provided in the layer of p-type material to form an array of n-p junctions therein, whereby a window is disposed to expose a portion of the circumscribed portion of p-type material for disposing an ohmic contact thereon.

27. A semiconductor material as claimed in one of claims 16 to 26, wherein a multi-wavelength detector is formed by:

interposing between the layer of p-type material and the passivation layer:

i. an isolating layer of p-type material;
ii. a second layer of p-type material; and
iii. another isolating layer of p-type material;

whereby the isolating layer surmounts the first layer of p-type material, the second layer surmounts the isolating layer, the other isolating layer surmounts the third layer, and the passivation layer surmounts the other isolating layer.

28. A semiconductor material as claimed in claim 27, wherein the semiconductor further includes a third layer, and a further isolating layer is interposed between the other isolating layer and the passivation layer in an accumulative manner, allowing the formation of additional wavelength detectors.

29. A semiconductor material as claimed in claim 27 or 28, wherein the layers of p-type material are each formed of a thickness corresponding to a predetermined cut-off wavelength.

30. A semiconductor material as claimed in any one of claims 27 to 29, wherein the semiconductor material is arranged such that incident light impinges on the substrate side.

31. A semiconductor material arranged as claimed in claim 30, wherein the thickness of each layer is such that the cut-off wavelength of the first layer is less than the second layer, and the second layer is less than any third layer, in like manner for any subsequent layers.

32. A semiconductor material as claimed in one of claims 27 to 31, wherein the isolating layers are formed of semiconductor material having a wider band gap than the semiconductor material used for forming the p-type layers.

33. A semiconductor material as claimed in one of claims 27 to 32, wherein the p-type layers and their surmounting isolating layers are arranged in pairs, such pairs being recessed in order that a portion of each corresponding p-type layer and isolating layer pair constitutes the final layer pair of that portion of the semiconductor material and is surmounted by said passivation layer.

34. A semiconductor material as claimed in claim 33, wherein a converted n-type region is formed in each final layer pair, such region extending through the isolating layer to the layer of p-type material; and windows being provided in

the passivation layer of each final layer pair in order to expose part of each converted n-type region for disposing ohmic contacts thereon.

35. A semiconductor material as claimed in claim 34, wherein a channel is formed extending through the outer layers of p-type material and the isolating material such that the passivation layer directly surmounts the first isolating layer at prescribed locations on the semiconductor material to divide the material into predetermined detector elements or pixels to constitute an array.

36. A semiconductor material as claimed in claim 33, wherein a converted n-type region is formed in each final layer pair, such region comprising:

the first p-type layer and the corresponding surmounting isolating layer thereof; and

the last p-type layer and the corresponding surmounting isolating layer thereof; whereby the converted n-type region extends through to the substrate, and windows are provided in the passivation layer of:

i. the first and last final layer pairs to expose part of each converted n-type region; and
ii. each final layer pair distant from the converted n-type region to expose part of the isolating layer in order to dispose the ohmic contacts on the exposed parts of the semiconductor material.

37. A semiconductor material as claimed in claim 36, wherein the converted n-type regions divide the semiconductor material into predetermined detector elements or pixels in order to constitute an array.

38. A semiconductor material as claimed in claim 34 or 36, wherein each detector element comprises a single final layer pair from each of the layers constituting

the semiconductor material, whereby each final layer pair is adjacent to another layer pair within the detector element.

39. A method for forming an automatically passivated n-p junction substantially as described herein in any one of the embodiments.

40. An n-p junction substantially as described herein in any one of the embodiments with reference to the drawings as appropriate.

41. A semiconductor body having an array of n-p junctions thereon substantially as described herein in any one of the embodiments with reference to the drawings as appropriate.

42. A semiconductor material having an n-p junction thereon substantially as described herein in any one of the embodiments with reference to the drawings as appropriate.